JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

Results for M.Tech (R13/R16) I Semester Regular/Supplementary Examinations December 2016

College: BHIMAVARAM INST. OF ENGG. & TECH. PENNADA, BHIMAVARAM:AP

Discrepancy pertaining to these results are to be submitted on or before 19-07-2017 with following documents at CE(PG) Office,JNTUK,Kakinada

- Online Registration Proof
- Hallticket
- DForm(Online)
- DForm(Offline)
- Attendance Sheet
- Any Other supporting Documents

Htno	Subcode	Subname	Internal	External	credits
13AP1D7007	G8205	DETECTION & ESTIMATION THEORY	34	19	0
13AP1D7009	G4503	ADVANCED DIGITAL SIGNAL PROCESSING	35	-1	0
13AP1D7009	G4505	STATISTICAL SIGNAL PROCESSING	38	-1	0
14AP1D5804	G0501	MATHEMATICAL FOUNDATIONS OF COMPUTER SCI	26	14	0
14AP1D5804	G0503	DATA BASE MANAGEMENT SYSTEMS	26	24	1
15AP1D5702	G5701	DIGITAL DESIGN USING HDL	33	25	1
15AP1D5703	G5701	DIGITAL DESIGN USING HDL	31	26	1
15AP1D5703	G6802	VLSI TECHNOLOGY AND DESIGN	36	11	0
15AP1D5704	G6806	DIGITAL SYSTEM DESIGN	29	28	1
15AP1D5705	G5701	DIGITAL DESIGN USING HDL	36	34	1
15AP1D5706	G5701	DIGITAL DESIGN USING HDL	35	35	1
15AP1D5706	G6802	VLSI TECHNOLOGY AND DESIGN	38	37	1
15AP1D5706	G6809	CMOS DIGITAL IC DESIGN	34	19	0
15AP1D5710	G5701	DIGITAL DESIGN USING HDL	31	-1	0
15AP1D5710	G6802	VLSI TECHNOLOGY AND DESIGN	36	11	0
15AP1D5710	G6806	DIGITAL SYSTEM DESIGN	27	-1	0
15AP1D7004	G6802	VLSI TECHNOLOGY AND DESIGN	29	18	0
15AP1D7005	G4503	ADVANCED DIGITAL SIGNAL PROCESSING	37	37	1
16AP1D5702	I5701	DIGITAL DESIGN USING HDL ELECTIVE 1	32	37	1
16AP1D5702	I5702	CPLD AND FPGA ARCHITECTURES AND APPLICAT	38	17	0
16AP1D5702	I5704	FRONT END VLSI DESIGN LABORATORY	39	55	1
16AP1D5702	I6801	DIGITAL SYSTEM DESIGN	28	27	1
16AP1D5702	I6802	VLSI TECHNOLOGY AND DESIGNELECTIVE 1	30	24	1
16AP1D5702	I6803	CMOS ANALOG IC DESIGN	38	3	0
16AP1D5702	I6806	CMOS DIGITAL IC DESIGN ELECTIVE 1	32	31	1
16AP1D5801	I0504	ADVANCED OPERATING SYSTEM	29	33	1
16AP1D5801	I0505	DATA WAREHOUSING AND DATA MINING	30	31	1
16AP1D5801	I4001	ADVANCED DATA STRUCTURES AND ALGORITHM A	28	24	1
16AP1D5801	I5801	MATHEMATICAL FOUNDATIONS OF COMPUTER SCI	33	29	1
16AP1D5801	I5802	COMPUTER ORGANIZATION AND ARCHITECTURE	27	33	1
16AP1D5801	I5803	DATABASE MANAGEMENT SYSTEMS	29	44	1
16AP1D5801	I5805	CSE LAB 1	35	55	1
16AP1D5802	I0504	ADVANCED OPERATING SYSTEM	35	24	1
16AP1D5802	I0505	DATA WAREHOUSING AND DATA MINING	36	24	1

Htno	Subcode	Subname	Internal	External	credits
16AP1D5802	I4001	ADVANCED DATA STRUCTURES AND ALGORITHM A	37	24	1
16AP1D5802	I5801	MATHEMATICAL FOUNDATIONS OF COMPUTER SCI	34	24	1
16AP1D5802	I5802	COMPUTER ORGANIZATION AND ARCHITECTURE	32	24	1
16AP1D5802	I5803	DATABASE MANAGEMENT SYSTEMS	34	31	1
16AP1D5802	I5805	CSE LAB 1	33	53	1
16AP1D5803	I0504	ADVANCED OPERATING SYSTEM	38	32	1
16AP1D5803	I0505	DATA WAREHOUSING AND DATA MINING	37	26	1
16AP1D5803	I4001	ADVANCED DATA STRUCTURES AND ALGORITHM A	37	28	1
16AP1D5803	I5801	MATHEMATICAL FOUNDATIONS OF COMPUTER SCI	39	33	1
16AP1D5803	I5802	COMPUTER ORGANIZATION AND ARCHITECTURE	37	30	1
16AP1D5803	I5803	DATABASE MANAGEMENT SYSTEMS	37	48	1
16AP1D5803	I5805	CSE LAB 1	37	57	1
16AP1D7001	I3801	SYSTEM DESIGN AND DATA COMMUNICATIONS LA	37	55	1
16AP1D7001	I4503	ADVANCED DIGITAL SIGNAL PROCESSING	26	5	0
16AP1D7001	I4504	DIGITAL DATA COMMUNICATIONS	27	24	1
16AP1D7001	I6801	DIGITAL SYSTEM DESIGN	26	6	0
16AP1D7001	I6802	VLSI TECHNOLOGY AND DESIGNELECTIVE 1	26	10	0
16AP1D7001	I8205	DETECTION AND ESTIMATION THEORY	28	14	0
16AP1D7001	I8206	OPTICAL COMMUNICATION TECHNOLOGY ELECTIV	27	-1	0
16AP1D7002	I3801	SYSTEM DESIGN AND DATA COMMUNICATIONS LA	38	53	1
16AP1D7002	I4503	ADVANCED DIGITAL SIGNAL PROCESSING	30	29	1
16AP1D7002	I4504	DIGITAL DATA COMMUNICATIONS	30	36	1
16AP1D7002	I6801	DIGITAL SYSTEM DESIGN	26	24	1
16AP1D7002	I6802	VLSI TECHNOLOGY AND DESIGNELECTIVE 1	27	32	1
16AP1D7002	I8205	DETECTION AND ESTIMATION THEORY	38	40	1
16AP1D7002	I8206	OPTICAL COMMUNICATION TECHNOLOGY ELECTIV	28	24	1
16AP1D7003	I3801	SYSTEM DESIGN AND DATA COMMUNICATIONS LA	37	52	1
16AP1D7003	I4503	ADVANCED DIGITAL SIGNAL PROCESSING	30	14	0
16AP1D7003	I4504	DIGITAL DATA COMMUNICATIONS	30	10	0
16AP1D7003	I6801	DIGITAL SYSTEM DESIGN	27	8	0
16AP1D7003	I6802	VLSI TECHNOLOGY AND DESIGNELECTIVE 1	27	7	0
16AP1D7003	I8205	DETECTION AND ESTIMATION THEORY	34	24	1
16AP1D7003	I8206	OPTICAL COMMUNICATION TECHNOLOGY ELECTIV	27	30	1
16AP1D7004	I3801	SYSTEM DESIGN AND DATA COMMUNICATIONS LA	37	52	1
16AP1D7004	I4503	ADVANCED DIGITAL SIGNAL PROCESSING	37	24	1
16AP1D7004	I4504	DIGITAL DATA COMMUNICATIONS	35	38	1
16AP1D7004	I6801	DIGITAL SYSTEM DESIGN	30	40	1
16AP1D7004	I6802	VLSI TECHNOLOGY AND DESIGNELECTIVE 1	27	27	1
16AP1D7004	I8205	DETECTION AND ESTIMATION THEORY	38	33	1
16AP1D7004	I8206	OPTICAL COMMUNICATION TECHNOLOGY ELECTIV	28	38	1
16AP1D7005	I3801	SYSTEM DESIGN AND DATA COMMUNICATIONS LA	39	58	1
16AP1D7005	I4503	ADVANCED DIGITAL SIGNAL PROCESSING	34	25	1
16AP1D7005	I4504	DIGITAL DATA COMMUNICATIONS	33	40	1
16AP1D7005	I6801	DIGITAL SYSTEM DESIGN	28	24	1
16AP1D7005	I6802	VLSI TECHNOLOGY AND DESIGNELECTIVE 1	27	4	0
16AP1D7005	I8205	DETECTION AND ESTIMATION THEORY	38	29	1
16AP1D7005	I8206	OPTICAL COMMUNICATION TECHNOLOGY ELECTIV	27	36	1

Note:1)For Recounting/Revaluation do the Online registration and send the total amount through online transfer
2)Take Seperate DD for the Challenge Valuation

**Note:1)For Recounting/Revaluation/Challenge By Revaluation Apply through Online(www.jntukresults.edu.in))

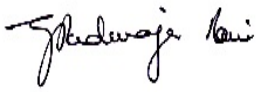
NOTE:2 [Last Date for Apply Recounting/Revaluation/Challenge By Revaluation: **26-07-2017]

**NOTE:3 [Please inform to the students to enter these subject codes for applying Recounting/Revaluation/Challenge By Revaluation]

**NOTE:
[-1 in the filed of externals indicates student absent for the respective subject.

-2 in the filed of externals indicates student result is withheld for the respective subject.

-3 in the filed of externals indicates Malpractice for the respective subject.]



Date:05-07-2017

Controller of Examinations